UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,128	02/09/2004	Chin-Cheng Chien	NAUP0552USA	2127

27765 7590 08/26/2005

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
AHMADI, MOHSEN	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,128	CHIEN ET AL.	
	Examiner	Art Unit	
	Mohsen Ahmadi	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-9,13,14 and 18-26 is/are rejected.

7)☐ Claim(s) 10-12, 15-17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Chin-Cheng Chien et al . For a "Method of Forming a Transistor Using Selective Epitaxial Growth" field February 09, 2004 has been examined.

Specification

The abstract of the disclosure is objected to because in paragraph (0017) line 2, the silicon substrate should be 50 instead of 10. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 18 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Ryu et al. (US Pat. 2002/0146888)

The present claims generally require a method of forming a transistor on a semiconductor substrate, the method comprising forming at least one gate structure on the semiconductor substrate, performing a surface cleaning process, the surface cleaning process comprising utilizing a chemical oxidation method for forming a first oxide layer on a surface of the semiconductor substrate not covered with the gate structure, and removing the first oxide layer, and utilizing a selective epitaxial growth method for forming a first epitaxial layer on the surface of the semiconductor substrate.

Regarding claim 1, Figure 1 of Ryu et al. discloses a single crystalline silicon substrate 10 comprising: a gate conductive layer 14, a gate insulating layer 12 and a capping insulating 16 are sequentially formed on a single crystalline silicon substrate 10 where a device isolation layer 11 is formed. Ryu et al. discloses a method of forming and removing a first oxide by performing a surface cleaning process and chemical oxidation method (See page. 2, paragraph [0021-0024]). Ryu et al. also discloses the method of selective epitaxial growth to form a first epitaxial on the surface of semiconductor substrate (See page. 2, paragraph [0025]).

Regarding claim 18, Figure 1 of Ryu et al. discloses a first region, a second region, and a mask layer covering the second region, where the first region is the epitaxial growth region said (a window on a semiconductor substrate), trench 11 is the second region and pattern 18 is the mask layer covering the second region. Ryu et al. also discloses a surface cleaning process with a hydrofluoric acid solution on the first region of substrate and forming an oxide layer and removing the oxide layer (See page. 1, paragraph [0014]). Ryu et al. also discloses, forming an epitaxial layer on the first region of the substrate (exposed region) (See page. 1, paragraph [0007]).

Regarding claim 26, Figure 1 of Ryu et al. shows wherein the mask layer (gate pattern 18) is a gate structure 18 that comprises a gate oxide layer 12 formed on a portion of the second region of the substrate (trench 11), a gate electrode 14 formed on the gate oxide layer 12, and a spacer formed on sidewalls 20 of the gate electrode 14.

Therefore, Claims 1, 18 and 26 are anticipated by the Ryu et al. reference.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 2, 3, 4, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al (US Pat. 2002/0146888).

Ryu et al. is relied upon as discussed above. Regarding claim 3, Ryu et al. discloses an oxidant acid as required by the chemical oxidation method to form the first oxide layer. Regarding claim 4, Ryu et al. discloses a diluted hydrofluoric acid as required to remove the first oxide (See page. 1, paragraph [0015]).

Regarding claims 2-4 and 8, Ryu et al. discloses all of the claimed features as stated above except for using the surface cleaning process repeatedly for removing a

first thickness of the semiconductor substrate, and the thickness of the layers which are removed.

Regarding claims 2, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use the cleaning process of Ryu et al. repeatedly because in general the transposition of process steps or the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, was held to not patentably distinguish the processes. Ex Parte Rubin, 128 USPQ 159 (1959). In the present case, the repetition of the cleaning process for its benefit, cleaning, would be obvious to one of ordinary skill in the art.

Regarding claim 8, it would have been obvious for one of ordinary skill in the art, at the time of the invention, to optimize the cleaning process of Ryu et al. and arrive at the claimed thicknesses. This accords with the rule that discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art. *In re Antoine* , 195 USPQ 6, (CCPA 1977). The amount of layer removed by the process of Ryu et al. is a matter of optimization and would be obvious to one of ordinary skill in the art. Moreover, with respect to the limitations of Claim 8, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *See Allen v. Coe*. 57 USPQ 136.

Claim 19, 20, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al (US Pat. 2002/0146888).

Ryu et al. is relied upon as discussed above. Regarding claim 20, Ryu discloses the surface cleaning process utilizes an oxidant acid to oxidize a surface of the first region to form the oxide (See page. 1, paragraph [0014]).

Regarding claim 24, Ryu et al. discloses a diluted hydrofluoric acid as required to remove the oxide layer (See page. 1, paragraph [0015]).

Regarding claim 25, Ryu et al. discloses the substrate is a silicon substrate, and the epitaxial layer is a silicon epitaxial layer utilizes (See page. 1, paragraph [007]).

Regarding claims 19, 20, 24 and 25, Ryu et al. discloses all of the claimed features as stated above except for using the surface cleaning process repeatedly for removing a portion of the substrate containing impurities.

Regarding claims 19, it would have been obvious to one of ordinary skill in the art, at the time of invention, to use the cleaning process of Ryu et al. repeatedly because in general the transposition of process steps or the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, was held to not patentably distinguish the processes. Ex Parte Rubin, 128 USPQ 159 (1959). In the present case, the repetition of the cleaning process for its benefit, cleaning would be obvious to one of ordinary skill in the art.

Claims 5, 6, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al (US Pat. 2002/0146888) in view of Yoo et al. (US 6,878,575).

Ryu et al. is relied upon as discussed above.

Regarding claims 5, 6, 21 and 22, Ryu et al. discloses all of the claimed features as stated above except for the sulfuric acid and hydrogen peroxide and the volume ratio sulfuric acid and hydrogen peroxide.

Regarding claims 5 and 21, Yoo discloses if organic pollutants are among the ingredients of the natural oxide layer formed on a surface of a semiconductor wafer, a predominant portion of such organic pollutants are removed through an SPM cleaning step using, for example, an acidic cleaning solution consisting essentially of sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2), and deionized water. (See column3, lines 15-22).

Regarding claims 6 and 22, Yoo discloses that the SPM cleaning stated above performed by mixing H_2SO_4 of about 98% (balance DI water) with H_2O_2 of about 30% in a volume ratio of about 2 to 4:1 and applying it to a substrate surface at a relatively high temperature above about 100° C (See col3, lines 29-34).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the cleaning solution as disclosed by Yoo in the cleaning process as disclosed by Ryu et al. for their known benefit in cleaning semiconductor substrates. As both references are drawn to the cleaning of semiconductor substrate using oxidant acid a *prima facie* case of obviousness is established.

Claim 7 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al (US Pat. 2002/0146888) in view of Twu et al (US Pat. 6,878,578).

Ryu et al. is relied upon as discussed above.

However, Ryu et al. doesn't disclose the sulfuric acid and ozone as required by claims 7 and 23.

Twu et al. disclose the formation of oxides on semiconductor substrates by chemical oxidation. Regarding claims 7 and 23, Twu et al. discloses that alternately, an ammoniacal hydrogen peroxide solution (SC-1), followed by DI water, may be used in place of ozone (See col 4, lines 4-12). Therefore, Twu et al. disclose the equivalence of ozone and hydrogen peroxide in the formation of oxides on semiconductor substrates.

It would have been obvious to one of ordinary skill in the art, at the time of invention, to substitute the hydrogen peroxide in the process of Ryu et al. with ozone for the benefit of forming oxides on semiconductor substrates, as Twu et al. disclose the equivalence of hydrogen peroxide and ozone. The substitution of one oxidant, ozone, for another, hydrogen peroxide, would be *prima facie* obvious to one of ordinary skill in the art.

Claim 9, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryu et al (US Pat. 2002/0146888) in view of Song et al. (US 6,580,134).

Ryu et al. is relied upon as discussed above. Ryu et al. also discloses forming a spacer 20, by anisotropically etching the insulating layer (See page. 2, paragraph [0021]. Furthermore, regarding claim 13, Ryu et al. discloses an ion-implantation process for forming a source electrode in the semiconductor substrate adjacent to one side of the gate structure and forming a drain electrode in the semiconductor substrate adjacent to another side of the gate structure where the gate pattern 18 referring to figure 1 is used as an ion-implantation, thereby forming an active region source and drain (See page. 2, paragraph [0021]).

Regarding claim 14, Ryu et al. discloses the method wherein the ion-implantation process is performed before the surface cleaning process is performed (See page. 2, paragraph [0021-0023]).

However Ryu et al. doesn't disclose the formation of a dielectric layer on the oxide layer to form the spacers as required by claim 9 and its dependent claims 13-15.

Regarding claim 9, Song et al. shows, in fig. 2, the gate structure comprises a gate oxide layer 104 on a portion of the semiconductor substrate 100, forming a gate electrode 106 on the gate oxide layer, forming a oxide layer 108 on the semiconductor substrate to cover the gate electrode, forming a dielectric layer on the oxide layer 108. An etching process is performed on the oxide layer and the dielectric layer to form a spacer on sidewalls of the gate electrode (See Col 4, lines 44-66). See fig. 3, wherein the gate structure comprises the gate oxide layer, the gate electrode, and the spacer.

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use an oxide layer and a dielectric layer as disclosed in the Song et al. reference, in the process of Ryu et al., for their known benefit in the art of forming spacers. The use of the dielectric layer and oxide layer in the spacers of Song et al., in the forming of the spacers of Ryu et al., is within the level of skill of one of ordinary skill in the art. The use of known material, dielectric and oxide layers, for its known purpose, forming of spacers, is a *prima facie* case of obviousness.

Allowable Subject Matter

Claims 10-12 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The cited prior art does not disclose the forming a second oxide layer on a surface of the gate electrode does not disclose as required by claim 10. With respect to Claim 15, the cited prior art does not anticipate or make obvious the ion-implantation process is performed *after* the first epitaxial layer is formed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is 1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00 am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA
August 22, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER